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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,229	MADDUX, JOHN T.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because

In Figs. 4 and 5, the sample positions (given only as "d" and a number) in the headings for each column of the tables apparently fail to properly distinguish between same-numbered sample points "d1" of different cycles, and thus the column headings give an incorrect description of how the invention could be implemented. The specification does not rectify the error in a consistent manner, as it describes and shows only six inputs to the edge detector (204 – Fig. 2), not enough to include "d1" from two different cycles at the same time. Based only on the description's repeated indications that only adjacent samples are compared in the edge detector, in Fig. 4, and within each individual cycle of Fig. 5, the sample "d1" in the first edge indicator "d1⊕d2" is presumably not the same "d1" used in "d6⊕d1". Because "d6" and "d1" samples taken in the same cycle, as apparently repeatedly described (with one exception, in paragraph [0020]) in the disclosure, would be non-adjacent, spurious edge detections and edge misses could result when the "d1" sample value in one cycle is not the same for "d1" in the next cycle. The decision matrix's ability to handle missed edges and multiple edges in a single cycle could compensate for the needlessly spurious edge detection implied by much of the disclosure, but there are apparent inconsistencies in the disclosure, nonetheless. It is therefor appropriate, to clarify the operation of the invention, that each "d" number should be associated with the correct cycle designation currently not

provided by the table headings. The examiner's suggestion here would be to substitute the legend "d1(t-1)" for the "d1" sample in the samples actually taken in the "previous cycle", "d1(t)" for the "d1" sample in the samples actually taken in the "current cycle", and so on for every sample point shown.

The Fig. 2 apparatus apparently requires non-described/non-shown storage elements and an additional sample output line for presenting seven samples, *i.e.* d1-d6 of one cycle (t-1) together with d1 of the next cycle (t), not six samples as described and shown. The Fig. 2 apparatus has an apparently needless delay -- a full cycle -- inherent in the edge-detection information convention using d1(t)⊕d2(t) and d6(t)⊕d1(t+1), instead of d6(t-1)⊕d1(t) and d5(t)⊕d6(t), for the first and last edge detections in each cycle. Fig. 2, therefor, does not appear at face value to be a serious attempt to represent a working apparatus.

The Fig. 5 edge detection arrangement, if realized with outputs of a parallel oversampler which is double the width of the parallel oversampler 202 shown in the single-cycle Fig. 2 apparatus, apparently requires a non-described decision delay of two full cycles, and an additional sampler output line for presenting 13 (not twelve, as described) samples necessary for obtaining all the edge detection outputs needed for each "two-cycle"-based decision by the decision matrix. One implication of the non-described and largely wasteful two-cycle delay is that there are non-described storage elements required between the parallel samples and the edge detector. Fig. 5 apparently shows a first edge being detected by d1(t-1)⊕d2(t-1) and a last edge by d6(t) ⊕d1(t+1), rather than showing a convention based on using d6(t-1)⊕d1(t) and

d5(t+1)⊕d6(t+1) for detecting the respective first and last edges. By applicant's convention, edge detection results using all the samples of the previous and current cycles must be held up for an edge detection that uses the first sample of the parallel twelve samples taken for the next two cycles, so that a complete set of thirteen samples needed to perform twelve edge detections is only made available to the edge detector a full two cycles after the "previous cycle" and "current cycle" samples are available. A full set of edge detections relevant to the same two cycles would be available two cycles sooner if the examiner's above-mentioned alternate convention – using d6(t-1)⊕d1(t) and d5(t)⊕d6(t) for the first and last edge detections -- was used instead, if the sampler output is fully parallel as suggested by the disclosure.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because the following changes are apparently necessary to correct incorrect, vague and/or confusing language:

> One aspect of the invention provides a novel scheme to improve channel jitter tolerance and perform data recovery across a serial data channel. In one implementation, the invention samples each data unit (cycle) in the data channel multiple times and, using two cycles, selects one of the samples as representative of the data bit or bits carried by the data unit. According to one aspect, the invention performs edge detection between adjacent data samples to determine the location of transitions between data units ~~(bits)~~. A representative data sample point is chosen which is as far away as possible from the detected edge and the next expected edge and is also adjacent to, or equal to, the expected ideal current sample point. According to another aspect of the invention, ~~as between two equally possible samples~~ given edges in a single cycle indicating two representative sample points, the algorithm selects the sample point within the current cycle which is furthest from the distribution of prior cycle edges.

Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

The specification apparently should be amended as follows:

> [0001] The invention pertains generally to serial data reception. More particularly, the invention relates to a method, apparatus, and system for extracting the correct data from a jittering data stream by using over-sampled data collected over two cycles.

[0002] In serial data communication systems a typical transmitting device generates pre-specified voltage levels at a particular frequency to transmit data to a receiving device over a transmission medium. A receiving device detects the voltage levels to determine the data being sent.

[0003] One common problem that affects serial communication systems is the noise and disturbances introduced into the transmitted signal. Such noise may cause jitter (a variation in the placement of data relative to the ideal location in time) and frequency offsets (a variation in the transmission frequency) which make it difficult to correctly ascertain the data transmitted.

[0004] FIG. 1 is a block diagram illustrating one embodiment of a system in which a device embodying a serial channel data recovery aspect of the invention may be employed.

[0005] FIG. 2 is a block diagram illustrating one embodiment of the serial channel data recovery aspect of the invention.

[0006] FIG. 3 is a diagram illustrating sampling of a serial data stream according to one aspect of the serial channel data recovery invention.

[0007] FIG. 4 is a matrix illustrating one embodiment of a single-cycle decision matrix used to select a data sample which is representative of a data unit ~~or bit~~.

[0008] FIG. 5 is a matrix illustrating one embodiment of a two-cycle decision matrix used to select a data sample which is representative of a data unit ~~or bit~~ according to one embodiment of the data recovery invention.

[0009] FIG. 6 is table illustrating the selection of samples under various edge ~~transition~~ location conditions according to one embodiment of the data recovery invention.

[0010] FIGS. 7-11 illustrate various conditions under which the data recovery aspect of the invention selects a data sample based on edge ~~transition~~ location information from two data units.

[0011] FIG. 12 is flow diagram illustrating a method of practicing data recovery according to one embodiment of the invention.

[0012] In the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, one of ordinary skill in the art would recognize that the invention may be practiced without these specific details. In other instances well known

methods, procedures, and/or components have not been described in detail so as not to unnecessarily obscure aspects of the invention.

[0013] Throughout this description the terms data unit~~,~~ and cycle~~, and/or bit may be~~ are used interchangeably to refer to a single data bit or other unit of data measure.

[0014] One aspect of the invention provides a data recovery algorithm which improves data extraction from a jittering and/or frequency-offset data stream by over-sampling the data stream, determining the ~~edges~~ edge closest to the expected ideal current sample point, and selecting the actual sample point based on the previous and current data unit ~~cycle~~ samples.

[0015] FIG. 1 illustrates a block diagram of a configuration of devices in which one embodiment of the invention may be employed. A first device (transmitter) 102 transmits serial data signals to a second device (receiver) 104 over a transmission medium 106. The transmission medium may be susceptible to noise or interference which may cause jitter and/or frequency offsets in the transmitted signal. The second device includes a data recovery or sampling point error correction component 108 embodying one or more aspects of the invention to improve data extraction.

[0016] The component 108 embodying one or more aspects of the invention may include one or more integrated circuit devices, circuit boards, software media, and/or other electronic devices. The component 108 may be part of a communication device, network device, computing device, processing device, and/or other types of electronic devices employing some form of serial communication.

[0017] FIG. 2 is a block diagram illustrating one embodiment of the data recovery component 108 embodying one or more aspects of the invention. Clock phase over-sampling may be employed to track the incoming serial data stream and extract the correct data. According to one implementation, the data recovery system 108 includes an over-sampler 202 to receive a serial digital data stream as input and provide two or more samples (i.e., d1-d6) per signal cycle or data bit. For the exemplary embodiment shown in FIG. 2 six data samples d1-d6 serve as inputs to an edge detector 204. The edge detector 204 detects ~~edge transitions~~ edge locations between adjacent data samples. This edge information is then provided to a decision matrix component 206 which selects the best point from which to ~~determine~~ sample the data unit or bit. A selector 208 may be coupled to the over-sampler 202 to receive the sampled data; the decision matrix component 206 then causes the selector 208 to output only that sample which the decision matrix 206 selects.

[0018] FIG. 3 provides an illustration of one embodiment of an incoming serial data stream (bit0, bit1, . . . , bit5) and six samples (six times over-sampling) for each data unit~~, bit, or cycle~~ or bit of the data stream. According to one implementation, six separate phases of a clock are used to independently sample the data stream.

[0019] Although for purposes of illustration FIG. 3 shows each data unit being sampled six times (six times over-sampling), the invention is not limited to a six time over-sampling scheme. A person of ordinary skill would appreciate that the invention may be practiced with fewer or greater number of samples per data unit. In various embodiments, a data unit may be sampled an even or odd number of times without departing from the invention.

[0020] The edge detector 204 attempts to find the ~~location~~ locations of the edges (i.e. low-to-high or high-to-low transitions) between data ~~bits~~ samples. In one implementation, the edge detector 204 extracts edge locations from the samples by XORing (performing exclusive OR logic operations on) ~~on~~ adjacent data samples. For the exemplary embodiment shown in FIG. 2, ~~six~~ seven samples serve as inputs to the edge detector 204 and the edge detector 204 generates six outputs, each output being obtained by XORing adjacent samples. For instance, in FIG. 3 for bit3, XORing of sample pairs d4 (between bit2 and bit3) and d5, d5 and d6, d6 and d1, d1 and d2, d2 and d3, and d3 and the next d4 (between bit3 and bit4) would provide the six outputs for the edge detector 204.

[0021] Throughout this description, the symbol $\oplus$ is employed to refer to a XORing (exclusive OR) operation or any collection of operations which provide an equivalent result.

[0022] For each cycle, the edge detector 204 generates the location where the ~~edges~~ edge occurred between samples. For example, if data sample d3 was logic low (0), and data sample d4 was logic high (1), the edge detector 204 would indicate an edge occurred between d3 and d4.

[0023] A decision matrix component 206 is coupled to the edge detector 204 to receive the outputs from the edge detector 204 and select one of the sample points according to a predefined decision algorithm, table, or matrix.

[0024] In the absence of jitter, the data edge would consistently be detected at the same location, for example d1$\oplus$d2. In the presence of jitter, however, over time the data edge location may move around. With a small amount of jitter, the edge may appear at two locations -- i.e. d1$\oplus$d2 and d2$\oplus$d3. With a larger amount of jitter, the edge may occur ~~across~~ at any one of four locations -- i.e. d6$\oplus$d1, d1$\oplus$d2, d2$\oplus$d3, ~~and~~ or d3$\oplus$d4.

[0025] FIG. 4 illustrates a single cycle decision matrix with six ~~possible~~ edge ~~transition~~ location inputs (d1⊕d2 . . . d6⊕d1) for the ~~`next`~~ current cycle and the ~~ideal~~ current state input. By locating ~~a transition~~ the edge and knowing the current ~~cycle~~ state, the `next` state is selected.

[0026] Note that throughout this description the terms `~~previous~~ current state`~~,~~ and `previously selected state`~~, and `previously selected sample`~~ are used interchangeably to refer to the state ~~or sample~~ selected in the previous ~~data unit~~ cycle. The terms `expected ideal sample`, `expected ideal sample point`~~,~~ ~~`ideal state`, `ideal current state`~~, and `expected ideal current sample` are used interchangeably to refer to the sample ~~or state~~ in the current ~~data unit~~ cycle which would be selected under ideal conditions. The expected ideal sample point is the data sample ~~or state~~ point which would be selected if no jitter occurs between the previous and current ~~data unit~~ cycles. If no jitter occurs between ~~data unit~~ cycles, the expected ideal data sample would be at the same location as in the previous ~~data unit~~ cycle. For example, if the ~~currently selected~~ current state is S1 (S1 was the selected state in the previous data ~~unit~~ cycle), s1 would be selected as the next state in the current ~~data unit~~ cycle under ideal conditions (no jitter).

[0027] Since FIG. 4 illustrates a single-cycle decision matrix, the closest edge ~~information~~ to the expected ideal sample point is not being used to determine the direction in which to shift to select the next state. For example, if the ~~ideal~~ current state ~~(corresponding to the previous selected state)~~ is S1, ~~edges~~ an edge at ~~that occur on~~ d5⊕d6 ~~are used to determine~~ determines the next state S2. But data samples d5 and d6 are the last two samples in the current cycle (data unit) and the expected ideal sample point corresponding to ~~ideal~~ current state S1 is the first sample point in the current cycle. Because of its long distance from the expected ideal sample point ~~S1~~ d1, the edge at d5⊕d6 in the current ~~data~~ cycle does not provide the most accurate or reliable ~~transition~~ edge from which to determine the next state.

[0028] However, the d5 and d6 samples from the previous ~~data unit~~ cycle are located closer to the expected ideal sample ~~state or~~ point ~~S1~~ d1. Hence, it would be better to use these earlier cycle samples to make a decision about the next sample point.

[0029] Because the samples d5 and d6 in the previous ~~data~~ cycle provide the closest edge to the expected ideal ~~state S1~~ sample point, they provide the most accurate and reliable information about the next state.

[0030] An aspect of the invention provides a decision matrix which is tolerant to high-frequency jitter.

[0031] One aspect of the invention provides a method or algorithm to select which of the data samples is the best sample to use for extracting the correct data from the data stream. One embodiment of this method is shown in FIG. 5 illustrating a decision matrix where two ~~data~~ cycles, the previous and current ~~data~~ cycles, and the ~~previous~~ previously selected state ~~(equivalent to the ideal sample point)~~ are employed by the decision matrix to select the best next ~~best~~ state.

[0032] The decision matrix contains a single ~~ideal~~ current state variable (S1 through S6) that ~~points to~~ indicates the sample point that is currently the best sample point (expected ideal sample point). For example, a state of s1 indicates that sample d1 is the best sample, s2 indicates d2 is the best sample, and so on. The decision matrix uses the ~~ideal~~ current state, one of S1 through S6, and the edge locations detected in the current and previous ~~data unit~~ cycles to determine the ~~next~~ best next state. As illustrated above, and explained in more detail below, the decision matrix seeks to determine the ~~next~~ best next state ~~by selecting~~ based on the closest ~~transition~~ edge to the expected ideal ~~current state~~ sample point from among the current and previous ~~data~~ cycles. Decision matrixes employing both the current and previous cycles improve jitter tolerance of an incoming serial data stream.

[0033] As illustrated in FIG. 5, for each of the six ~~ideal~~ current states there are five ~~edges~~ edge locations that are used to determine what the next state will be. For examples, if the current state is S6, then the edges generated by the previous cycle samples d4⊕d5, d5⊕d6, by the previous cycle sample and current cycle sample ~~and~~ d6⊕d1, and by the current cycle samples d1⊕d2 and d2⊕d3 will be used to determine the next state.

[0034] Referring to FIG. 6, if no edge is detected on any of these five ~~edges~~ edge locations then no state change is made~~; the next state is the ideal state (equivalent to the previously selected state)~~. If a single edge is detected on one of these five ~~edges~~ edge locations, then the next state is determined by that edge. If more than one edge is detected on more than one of these five ~~edges~~ edge locations and they all ~~generate~~ indicate the same next state, then that next state will be used. Finally, if more than one edge is detected on more than one of these five ~~edges~~ edge locations and the next state ~~generated~~ indicated by these edges are different, then there is a conflict and the next state will be the same as the ~~ideal~~ current state ~~(equivalent to the previously selected state in the previous data unit cycle)~~.

[0035] According to another implementation, if more than one edge is detected and different states are ~~generated~~ indicated, then the state which was ~~generated~~ indicated by the most number of edges is selected as the next state. For

example, if two edges ~~generate~~ indicate state s1 and one edge ~~generates~~ indicates s2, then the next state will be s1.

[0036] In more detail, referring to FIG. 7, if the ~~ideal~~ current state ~~or sample~~ is S6 and d5⊕d6 is true (an edge ~~transition~~ was detected) but no other edges were detected, then the next state is s1. Similarly, referring to FIG. 8, if the ~~ideal~~ current state is S6 and d2⊕d3 is true and no other edges were detected, then the next state is s5. Also, if the ~~ideal~~ current state is S6 and both d2⊕d3 and d1⊕d2 are true, the next state is s5. However, if the ~~ideal~~ current state is S6 and both d5⊕d6 and d2⊕d3 are true, then there is a conflict and the next state will stay at s6.

[0037] Thus far, the next state has been selected from among the two states adjacent to the ~~ideal~~ current state or the ~~ideal~~ current state itself. For example, if the ~~ideal~~ current state is S2, then the next state will be either s1, s2, or s3 as determined by the matrix. Additionally, a study of the exemplary matrix in FIG. 5 discloses that the next state is chosen to have the location of its expected ideal sample point be as far as possible from the detected edge and the next expected edge and ~~yet~~ also adjacent to, or equal to, the ~~ideal~~ location of the expected ideal sample point for the current state. That is, the decision matrix is coded so that the state pointer to next state moves away from ~~the~~ selecting representative data samples that are close to an edge. A ~~state or~~ sample point is selected which lies substantially midway (or moves in the direction of the mid-point) between the detected edge and the next expected edge and ~~yet~~ is also adjacent to, or equal to, the location of the expected ideal sample point for the ~~ideal~~ current state. Note that for a system which samples each data unit (bit) N times (where N is an integer value), the next edge is expected to lie a distance of N samples from the detected edge. In the examples of FIGS. 7 & 8 the value of N is six since each data unit is sampled six times, at different ~~locations or~~ points.

[0038] For example, referring to FIG. 9, if the ~~ideal~~ current state is S2 and the only edge detected is at d5⊕d6 (either in the previous cycle or next cycle), then, state s2 is selected since ~~it~~ d2 lies at the midpoint between the two edges (previous d5 and current d5). Note that in this example, the edge is assumed to lie at d5; since d2 is equidistant between two d5 samples, ~~s2~~ d2 is selected as the best ~~state or~~ sample. Similarly, referring to FIG. 10, if the ~~ideal~~ current state ~~or sample~~ is S2 and the only edge detected is at d6⊕d1 or d1⊕d2, then the next state ~~or sample~~ is selected to be s3 since ~~it~~ d3 is the furthest ~~state or~~ sample from ~~s6~~ d6 or ~~s1~~ d1, respectively, yet adjacent to ~~s2~~ d2. Also, referring to FIG. 11, if the ~~ideal~~ current state ~~or sample~~ is S2 and the only edge detected is at d3⊕d4 or d4⊕d5, then the next state ~~or sample~~ is selected to be s1 since ~~it~~ d1 is the ~~furthers~~ furthest ~~state~~ from ~~s3~~ d3 or ~~s4~~ d4, respectively, ~~yet~~ and is adjacent to the expected ideal current ~~state S2~~ sample point d2.

[0039] A person of ordinary skill in the art would recognize that decision matrixes for any number of states may be created as described above.

[0040] A conditional state occurs where two states are equally likely under the algorithm described above. For example, if the ~~ideal~~ current state is S2 and d2⊕d3 is the only edge, then s3 and s1 are equally likely. According to one implementation, one of the two possible states is chosen arbitrarily when this condition occurs.

[0041] Another aspect of the invention provides a method, system, or algorithm to decide between two equally likely states. That is, where a conditional state occurs (i.e., where both s1 and s3 are equally likely) then the decision matrix looks at the distribution of previous edges to select the best next state from among the two choices. ~~As between~~ Given two possible next states, the algorithm selects the state with an expected ideal sample location that ~~which~~ is furthest from the distribution of prior cycle edges.

[0042] For example, in a low jitter channel edges may occur only on d1⊕d2 and d2⊕d3. Based on the decision matrix in FIG. 5, with edges only at d1⊕d2 and d2⊕d3 the state pointer will converge and alternate between s4 and s5. Assuming the incoming jitter increases, transitions may now occur across four edge locations, i.e. d6⊕d1, d1⊕d2, d2⊕d3, and d3⊕d4. If at least three d6⊕d1 edges in a row occur, the state pointer either will move from s4 to s3 or from s5 to s4 and then to s3 ~~(depending on whether it started in s5 or s4)~~. In either case the current state pointer will be S3 and the previous state will be S4. With the current state of S3, if the next edge detected is d3⊕d4 then the next state is either s2 or s4. However, it is undesirable to select s2 because data sample d2 is ~~right in the middle of~~ centrally overlapped by the distribution of edges -- recent edges were on d6⊕d1, d1⊕d2, d2⊕d3, and d3⊕d4. The fact that d2 is ~~located in the middle of~~ centrally overlapped by the distribution of recent previous edges ~~(or within the distribution of previous edges)~~ increases the likelihood that s2 may be an erroneous reading. Rather, an algorithm of the invention would select s4 as the next state in this case. State s4 is more desirable than s2 because data sample d4 ~~is on~~ overlaps the far right-hand ~~edge~~ end of the distribution of recent edges and is more likely to have the correct data. According to one implementation, state s4 would be selected since the previous state was s4. That is, ~~as between~~ given two possible states (i.e., s2 or s4) the algorithm would select the state which was most recently selected in previous data cycles. In the example above, previous states would include S5, S4, and S3, from earliest to most recent, in that order. ~~As~~ Given a choice between states s2 and s4, state s4 was most recently selected so it would be selected in this case.

[0043] In another example, if a transition is detected at d1⊕d2 in ~~(~~current state S1~~)~~ the two possible states are s2 or s6. If the previous states include, from earliest to most recent, S3, S2, S1, S6, and S1, then s6 would be selected as the best next ~~best~~ state ~~or sample~~ since, as with the choice between ~~S2~~ s2 and ~~S6~~ s6, ~~S6~~ s6 was the most recently selected state.

[0044] Thus, where a choice must be made between two possible states, the invention selects the most recent state to have been selected from among the two possible states or, equivalently, ~~select~~ selects the state with an expected ideal sample point located ~~furthest from~~ closest to the midpoints between the most recent previous edges (or the distribution of previous edges). Such a selection algorithm has shown to increase jitter tolerance of an incoming serial data stream. In one implementation, the invention may retain memory of the previous M selected states so that a decision between two possible states may be made. In various implementations, the number of previous edges employed to make such decision may vary.

[0045] FIG. 12 illustrates one method of practicing the data recovery aspect of the invention. Each data unit (bit) across a serial data channel is sampled multiple times, at different locations along its cycle 1202. These samples are then employed to determine edge ~~transitions~~ locations between adjacent data samples 1204. One of the data samples is then selected as representative of a data unit based on the edge ~~transition~~ information for two data units/cycles (i.e. the current data cycle and the previous data cycle) 1206.

[0046] According to one implementation, the serial data stream received by a device embodying the invention may be a Universal Serial Bus (USB) compliant data stream, a Serial Advanced Technology Attachment (ATA) compliant data stream, and~~/or~~ many other types of serial communication channels.

[0047] A person of ordinary skill in the art would recognize that there are other benefits to the invention herein disclosed. For example, while some data recovery systems may gather edge information over five (5) cycles and perform a histogram of this data to determine an optimal sample point, such architecture must store much more information than the disclosed approach. Because the invention need not store as much information as other data recovery systems, it can be implemented in a smaller area of silicon (in a chip) since less transistors are employed.

[0048] Greater or fewer sampling points may be employed in different embodiments without deviating from the invention. Although some exemplary embodiments of the invention have employed six-times (6 x) over-sampling for purposes of illustration, the disclosed invention may be implemented at any other level of over-sampling without deviating from the invention.

[0049] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art. Additionally, it is possible to implement the invention or some of its features in hardware, programmable devices, firmware, software or a combination thereof. The invention or parts of the invention may also be embodied in a processor readable storage medium or machine-readable medium such as a magnetic, optical, or semiconductor storage medium.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. Claims 1, 2, 4-23 and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,598,446 to Van Der Tuijn (hereafter referred to as Van Der Tuijn).

Van Der Tuijn discloses clock signal extraction arrangements for sampling a signal from, *e.g.* a cordless telephone, thereby "receiving a serial data stream". Received digital data is oversampled (col. 20, line 64-67) in Van Der Tuijn's preferred embodiment. In one embodiment disclosed by Van Der Tuijn (col. 4, lines 55-56), "N" = 6-times oversampling is used for "sampling each data unit in the data stream N times, and at different locations along each data unit, to obtain multiple data samples per data unit". Edges between adjacent samples in Van Der Tuijn's arrangements are detected (col. 2, lines 52-55) in the oversampled data by an edge detector 41. A sample is selected by the extracted clock (col. 4, lines 61-67) in Van Der Tuijn's arrangements. In Van Der Tuijn's preferred embodiment, the phase of the extracted

clock signal is varied based on the center between each pair of consecutive edges. Variations in the positions of a number of centers are averaged to produce a phase error. In Van Der Tuijn's preferred embodiment the current center and an immediately previous center are used to produce the phase error, and the phase of the extracted clock signal is changed an amount equal to the phase error (col. 1, lines 42-57). Accordingly, Van Der Tuijn's sample selection is "based on the location of edges over the current and previous data units". With Van Der Tuijn's arrangements, the center between each pair of consecutive edges is determined by counting a number of cycles of an oversampling signal which occur between each pair of consecutive edges to obtain a bit width. The bit width is divided in half and the result added to an edge phase value to obtain a value for the center. Accordingly, Van Der Tuijn's sample selection is also based on "the location of an expected ideal data sample".

Regarding claims 2 and 16, as the edges preceding and following the center are considered in Van Der Tuijn's sample selection, the "closest" edges determine the center and thus determine the "expected ideal data sample".

Regarding claims 4 and 14, ideally, there is no jitter, the centers do not move and so maintain an "N" sample spacing.

Regarding claims 5, 17, 19 and 32, when the correction window in Van Der Tuijn's arrangements is one (col. 7, lines 9-15), the representative sample timing can only shift by one sample position among the oversampled data from one cycle to the next.

Regarding claim 6, as mentioned above with regard to phase error determination in Van Der Tuijn's arrangements, sample selection can be based on the most recent two cycles of oversampled data.

Regarding claims 7 and 18, with Van Der Tuijn's arrangements, a pair of missing edges would apparently result in no change to the selected sample timing, resulting in no change from the "expected ideal" representative sample position for the cycle.

Regarding claims 8, 19 and 33, with Van Der Tuijn's arrangements, a missing edge at the end of a cycle would apparently result in no change to the selected sample timing, which would be referenced from the leading edge of a previous cycle.

Regarding claims 9, 10, 20 and 21, detecting regularly-spaced "multiple edges" with Van Der Tuijn's arrangements, *i.e.* regularly-spaced starting and ending edges for multiple data units, results in regularly spaced and centered representative samples.

Regarding claims 12 and 23, when the bit width is an even number of samples, there are two samples that are equally centered within the bit width, and the earlier of the two is apparently preferred by Van Der Tuijn's arrangements (see *e.g.* interval "BIT 2", Fig. 4).

Claim Rejections - 35 USC § 103

5. Claims 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Der Tuijn.

Van Der Tuijn does not disclose using software instructions to implement the logic operations described for his sample selection arrangements. Official Notice is

given that the advantages of implementing logic operations by using a programmed computer, including low cost, ease of distribution and modification, hardware development design emulation/simulation, etc., were well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Van Der Tuijn's logic operations using a programmed computer. Such an implementation would have been obvious because the advantages of implementing logic operations by using a programmed computer, including low cost, ease of distribution and modification, hardware development design emulation/simulation, etc., were already well known.

Response to Arguments

6. Applicant's arguments filed 13 June 2005 have been fully considered but they are not persuasive.

Regarding the objections to the specification, applicant's decision to leave the specification with needlessly confusing and misdescriptive language is, of course, not well taken for reasons that should be patently clear to any competent practitioner.

Applicant's decision to interpret "oversampling" as something other than sampling at more than one point per data unit is, of course, wholly inconsistent with the well-known meaning of "oversampling."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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smb